
Subject: Homebrew expansion RAM

Posted by [nessus](#) on Thu, 30 May 2013 03:58:06 GMT

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Organization: The Patriarchy of Kzin

Lines: 100

*** REPLACE THIS LINE WITH YOUR MESSAGE ***

1 +5V Power +5V Power for Speech Synthesizer
2 SBE Output SPEECH BLOCK ENABLE CPU read from 90XXH
or CPU write to 94XXH
3 RESET/ Output System reset
4 EXTINT/ Input EXTERNAL INTERRUPT User/expansion int.
5 A5 Output Address Bit 5
6 A10 Output Address Bit 10
7 A4 Output Address Bit 4
8 A11 Output Address Bit 11
9 DBIN Output DATA BUS IN Hi=CPU read
10 A3 Output Address Bit 3
11 A12 Output Address Bit 12
12 READY Input Set READY=Lo for wait states
13 LOAD/ Input Causes CPU to fetch new Program Counter
& Workspace pointer from FFFCH & FFFEh
14 A8 Output Address Bit 8
15 A13 Output Address Bit 12
16 A14 Output Address Bit 12
17 A7 Output Address Bit 7
18 A9 Output Address Bit 9
19 A15/CRUOUT Output Address Bit 15/CRU Data out(LS Address bit)
20 A2 Output Address Bit 2
21 GND Ground Ground reference
22 CRUCLK/ Output CRU strobe
23 GND Ground Ground reference
24 PH3/ Output 3MHz clock
25 GND Ground Ground reference
26 WE/ Output CPU write
27 GND Ground Ground reference
28 MBE/ Output DSR access 4000H->5FFFH
29 A6 Output Address Bit 6

- 30 A1 Output Address Bit 1
- 31 A0 Output Address Bit 0(MS Address bit)
- 32 MEMEN/ Output Memory access
- 33 CRUIN Input CRU read data
- 34 D7 Bidirectional Data Bit 7(LS Data bit)
- 35 D4 Bidirectional Data Bit 4
- 36 D6 Bidirectional Data Bit 6
- 37 D0 Bidirectional Data Bit 0(MS Data bit)
- 38 D5 Bidirectional Data Bit 5
- 39 D2 Bidirectional Data Bit 2
- 40 D1 Bidirectional Data Bit 1
- 41 IAQ Output Instruction Acquisition Cycle
- 42 D3 Bidirectional Data Bit 3
- 43 -5V Power -5V Power for Speech Synthesizer
- 44 AUDIO IN Input User Audio input to sound generator

Gotchas:

1. EVERY memory access consists of 2 sequential 8-bit accesses with odd (MS) byte written or read first.
2. A0 is MOST SIGNIFACANT address bit.
3. D0 is MOST SIGNIFICANT data bit.

| CPU Address | INT RAM | EXP RAM | BUS BUF | EXP Address | Remarks |
|--------------|---------|---------|---------|--------------|---------------------------------|
| 0000 -> 1FFF | Off | Off | Off | --Not Used-- | Console ROM Access |
| 2000 -> 3FFF | Off | On | On | 0000 -> 1FFF | Low EXP RAM Access |
| 4000 -> 5FFF | Off | Off | On | --Not Used-- | DSR ROM Access |
| 6000 -> 7FFF | Off | Off | Off | --Not Used-- | Cartridge Access |
| 8000 -> 9FFF | On | Off | Off | --Not Used-- | INT RAM/VDP/Speech Synth Access |
| A000 -> BFFF | Off | On | On | 2000 -> 3FFF | High EXP RAM Access |
| C000 -> DFFF | Off | On | On | 4000 -> 5FFF | High EXP RAM Access |
| E000 -> FFFF | Off | On | On | 6000 -> 7FFF | High EXP RAM Access |
| 0000 -> 1FFF | Off | Off | Off | --Not Used-- | CRU Access |

Data Path:

